## IN THE CLAIMS

## 1-10 (canceled)

- 11. (currently amended) A fast data access circuit having an input clock signal and an input data burst signal comprising a plurality of data bits, the input clock signal having a frequency, the circuit comprising:
  - a mode/configuration register for generating a mode control signal in response to a loaded configuration word comprising at least one mode control bit and at least one clock frequency selection bit that is set in response to the input clock signal frequency;
  - a clock delay circuit coupled to the input clock signal and the mode/configuration register, the clock delay circuit providing, in response to the at least one clock frequency selection bit, a selectable time delay to the input clock signal to produce a delayed clock signal such that the time delay is smaller for higher input clock signal frequencies;
  - a multiplexing circuit having a first input coupled to the input clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal;
  - control logic for generating a plurality of register control signals in response to the selected clock signal; and
  - a data first-in-first-out register, coupled to the control logic and the input data burst signal, for outputting each of the plurality of data bits at a rate selectable by bit in response to the plurality of register control signals.
- 12. (Original) The circuit of claim 11 wherein the clock delay circuit comprises a plurality of delay circuits each coupled to a selection circuit, each selection circuit being coupled to the at least one clock frequency selection bit.

- 13. (Original) The circuit of claim 12 wherein each of the plurality of delay circuits comprises a plurality of inverter gates.
- 14. (currently amended) A memory device comprising:
  - an array of memory cells for storing a plurality of data bits;
  - a clock input for accepting a clock signal; and
  - a fast data access circuit comprising:
    - a clock delay circuit that generates a delayed clock signal, from a plurality of selectable time delays, in response to the clock signal and a delay control signal;
    - a control circuit that generates a mode control signal and the delay control signal;
      a multiplexing circuit having a first input coupled to the clock signal and a second
      input coupled to the delayed clock signal, the multiplexing circuit
      outputting a selected clock signal in response to the mode control signal;
      and
    - control logic for generating data output register control signals in response to the selected clock signal; and
    - a <u>first-in-first-out</u> data output register, coupled to the <u>data output register control</u>

      <u>signals</u> multiplexing circuit and the array of memory cells, for outputting
      the plurality of data <u>bits</u> bit at a data rate determined by the selected clock
      signal.
- 15. (Original) The memory device of claim 14 and further including a burst counter for generating a plurality of sequential addresses, within a predetermined address range, to the array of memory cells such that a plurality of data is accessed within the predetermined address range.

16-17 (canceled)

- 18. (currently amended) An electronic system comprising:
  - a processor that generates control signals; and
  - a memory device for storing and accessing data in response to the control signals, the device comprising:
    - an array of memory cells for storing a plurality of data bits;
    - a clock input for accepting a clock signal; and
    - a fast data access circuit <u>coupled to the array of memory cells</u>, the circuit comprising:
      - a clock delay circuit that generates a delayed clock signal, from a plurality of selectable time delays, in response to the clock signal and a delay control signal;
      - a control circuit that generates a mode control signal;
      - a multiplexing circuit having a first input coupled to the clock signal and a second input coupled to the delayed clock signal, the multiplexing circuit outputting a selected clock signal in response to the mode control signal; and
      - a data output register, coupled to the multiplexing circuit and the array of memory cells, for outputting the plurality of data bit at a data rate determined by the selected clock signal.
- 19. (currently amended) A method for performing fast data access in a memory device comprising an array of memory cells, the method comprising:
  - generating a delayed clock signal from an input clock signal such that the delay is selected from a plurality of delays in response to a control input;
  - selecting between the input clock signal and the delayed clock signal to generate a selected clock signal;
  - generating a plurality of data output register control signals in response to the selected clock signal;
  - storing transferring a plurality of data bits from the array of memory cells to a <u>first-in-first-out</u> data output register; and

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accessing outputting the plurality of data bits from the data output register at a rate determined by the plurality of data output register control signals.

- 20. (Original) The method of claim 19 wherein the control input is a configuration word loaded into a mode/configuration register.
- 21. (Original) The method of claim 19 and further comprising receiving a configuration word comprising at least one bit indicating a fast data access mode and at least one bit indicating a frequency of the input clock signal.
- 22. (currently amended) A method for performing fast data access in an electronic system including a memory device comprising an array of memory cells, the method comprising: generating a configuration word incorporating at least one mode select bit and at least one clock frequency indication bit;

loading the configuration word into a mode/configuration register;

- generating a delayed clock signal from an input clock signal such that the delay is selected from a plurality of delays in response to the at least one clock frequency indication bit;
- selecting between the input clock signal and the delayed clock signal, in response to the at least one mode select bit, to generate a selected clock signal;
- generating a plurality of data FIFO register control signals in response to the selected clock signal;
- storing a plurality of data bits from the array of memory cells to a data FIFO register; and accessing outputting the plurality of data bits from the data FIFO register at a rate determined by the plurality of data FIFO register control signals.